Technical Symposium

Application Oriented Unipolar SiC Switching (Invited) Devices
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High Power SiC Diodes: Characteristics, Reliability, (Invited) and Relation to Material Defects
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Low Resistivity Ohmic Contacts Sequentially (Invited) Formed in n- and p-type Regions on the Same 4H-SiC Substrate
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Application oriented unipolar SiC switching devices

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Following industries dreams of solid state power devices, an ideal switch with zero static and zero dynamic losses and a price close to electromechanics should be created with silicon carbide. Nice dreams, of course, this is not even visible at the horizon of ten years or more. However, this kind of thinking strongly influences the decisions whether silicon carbide has a successful future or is intended to end with glory. Thus, it is necessary to approach these demands as close as possible in order to get over the barrier existing for the introduction of a new and on a first glance much more expensive material concept.
Principally, there are two ways to do this. Firstly, one can look for an application were today's devices are not able to fulfill the requirements (e.g. high voltage, high current and high switching speed). In these fields, however, the margins are probably large, but the number of necessary devices is so small, that it becomes hard to find manufacturers which are willing to take over the investment for a fabrication since SiC despite its technological vicinity to silicon does not match to any existing production line. The second way is to look for applications with valuable system advantages and high volume. Also if these two items are often contrary, there seems to be a special kind of SMPS (Switch Mode Power Supplies) topologies which can probably serve similar to the PFC (Power Factor Corrector) as a driver for the introduction of SiC Schottky diodes as the entry for SiC switches into mass production. In such applications, low currents in the range of some amps and high switching speeds combined with blocking voltages above 1000V are recommended. Since in addition, the control power should be comparable to conventional devices like MOSFETs or IGBTs , the talk will outline that currently, the solution in silicon carbide represents a unipolar switch. In order to keep the costs as small as possible, the specific on-resistance must be as low as possible for small consumption of SiC area. However, thermal considerations must not be neglected at all since with smaller total device areas the thermal resistance increases.
In order to realize such a device, the first approach could be a MOSFET like structure. However, attempts to realize a powerful MOSFET in silicon carbide are still not successful due to interface and reliability problems which will be thoroughly discussed /1,3/. Bipolar devices with an non-even number of pn-junctions exhibit unacceptable high threshold voltages while the classical bipolar transistor (even with a current gain of 20) is not easy to control powerless and can't be paralleled easily. Thus, we currently favor the JFET concept in connection with a low voltage silicon power MOSFET presented as published earlier /2,4/. Up to now, we have two JFET configurations investigated, one type with extremely small on-resistance but limited switching speed and a second type with superior switching speed on the costs of a nearly doubled specific on-resistance. Figure 1 compares the turn-off for both devices as an indicator for the switching speed. As a good indicator for the dynamic performance serves the potential at the MOSFET drain during the transient phase. It can be seen that for the first type (left graph), the voltage at the MOSFET drain increases up to ist avalanche. This is due to an RC delay caused by the high p-type resistance in the buried p-layer. In the second type (right graph), the p-gate has everywhere an ohmic connection to the gate metallisation layer. Thus, the device is able to turn off very fast. In fact, the measurements show that for the second type the switching speed of the complete circuit is nearly independent on the JFET and can be influenced by a proper choice of the MOSFET. Possible future

structures with special respect to switching speed, overload behavior and still lower specific on-resistances will be discussed at the conference.

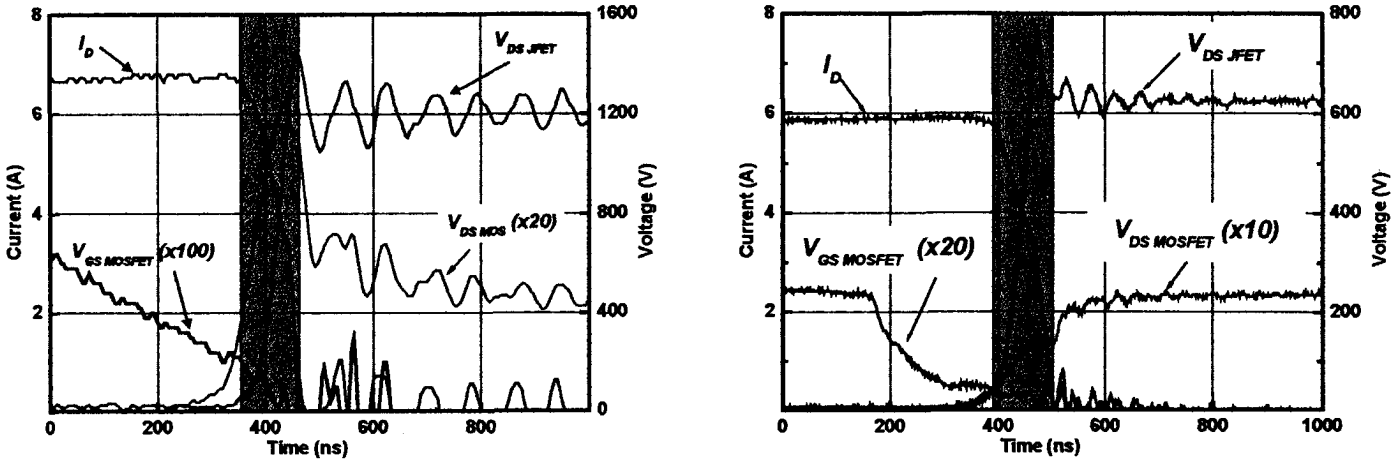

Figure 1: Turn off behavior of a Si MOSFET/ SiC JFETcascode with unsatisfactory dynamics (left) and the fast type (right), in a chopper circuit with clamped inductive load

A further item worth to discuss is the question what will follow such a device with broad application. Often high voltage applications with blocking voltages exceeding 3kV are mentioned. However, still open is the question of the upper limit for unipolar devices with respect to their blocking voltages. Recently, we have fabricated 3,5kV JFETs with a specific on-resistance of only 26mΩcm^2. We believe that these results will further shift the introduction of bipolar SiC-devices to blocking voltages of about 6,5kV or even higher since it now becomes possible to implement fast unipolar switches in high voltage applications. Additionally, with respect to bipolar SiC-devices, the problem of the poor p-type conductivity in epilayers as well as in the substrate is a hurdle hard to overcome in the near future. Thus, the unipolar SiC device concept will be most suited at least the next generations of silicon carbide power devices.

Acknowledgement

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High power SiC diodes: Characteristics, Reliability, and relation to material defects

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One of the most important device applications for SiC is for high power unipolar and bipolar devices. In this paper we present state-of-the-art results and performance of unipolar Junction Barrier Schottky (JBS) diodes intended for the voltage range of 600-3300V and for bipolar PiN diodes for the range between 3kV and 6 kV.

JBS diodes with 1200 V blocking voltage show a forward voltage drop of 1.25 V at 5.2 A (100A/cm^2) and 1.5V at 10A at 30°C. For 125°C, the voltage drop increases to 1.3 and 1.7 V, respectively. The diodes sustained surge currents of 2000A/cm^2 and show stable avalanche in reverse direction. Reliability tests of over 3000h for reverse bias and frequency operation proved stable parameter values for all diodes. The epitaxial design for the JBS diodes can be done for 80% critical electric field, while Schottky diodes have shown blocking voltages corresponding to only 70% of the theoretical junction field strength. This results for the JBS diode in a lower on-resistance than a Schottky diode on the same wafer despite the extra resistive contribution from the integrated p-grid (Fig. 1,2).

PiN bipolar diodes for 4.5kV using different anode technologies proved, that ideal on-state voltages of 3.1V at 100A/cm^2 can be achieved. Using a balance between epitaxial and implanted emitters, a speed-to-forward voltage trade-off can be implemented similar as in advanced Si devices. Using such chips (5mm edge length) power modules were assembled connecting 8 diodes in parallel. Switching tests for power ratings of about 1MW were made with 200ns turn-off operations of 300A against 3000V with 3800V peak voltage at the SiC diode. Blocking reliability of such diodes was also proven to be stable over > 5000h and unaffected by screw dislocations or other structural crystal defects. Other reliability functions such as frequency switching, surge current pulses, reverse avalanche stability as well as the cosmic ray failure rate testing, were executed according to power devices standards and did not show any concern (Fig. 3, 4).

However, bipolar SiC devices exhibit an increase of the conducting state characteristics called "forward degradation" (Fig. 5). An extremely wide statistic ranging from stable elements to such shifting their forward voltages more than 15V, during time spans of milli-seconds to kilo-hours are observed for nominally identical devices. The phenomenon was first observed by us. Since then have identified the cause as recombination-enhanced movement of dislocations, forming extended single stacking faults (SF) in the epitaxial layer. Electrically these SF decrease the carrier lifetime and create barriers for the current flow. The SFs are nucleated at dislocations present in the virgin material. Identification was carried out and densities were mapped over entire wafers. It is shown that at least some of the several different types of observed dislocations, including basal plane dislocations are actually present in the wafer substrate and cannot be eliminated at the substrate epi interface. Mature processing induces no additional faults in the epitaxial layer. However, continued material development must significantly reduce these dislocations, as well as the conventional crystal defects, before bipolar devices will achieve stable device operation.

Unipolar SiC devices for 300-2000V

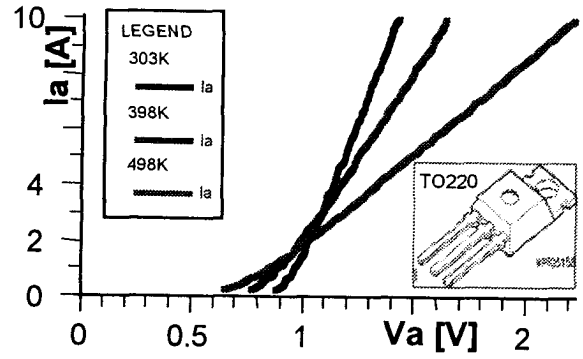

Figure 1 Measured forward characteristic of JBS diodes for 1200V for RT-225C. The device area is 5.2mm^2.

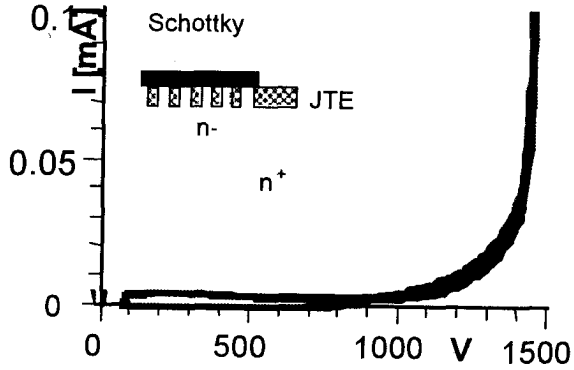

Figure 2 Reverse characteristic of the diode in Fig.1. The inset shows the diode cross-section with ca. 4um schottky spacing.

Bipolar SiC devices for over 3000V

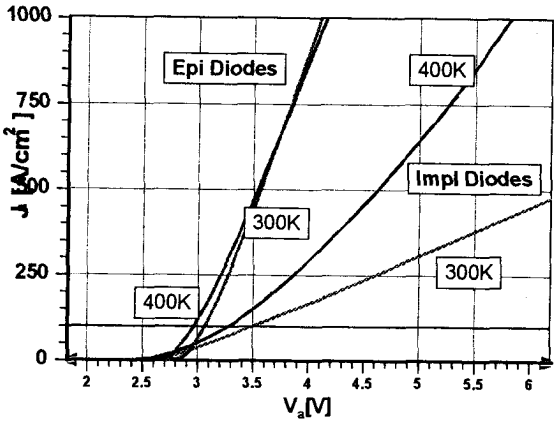

Figure 3 Measured on-state characteristic of bipolar diodes for 4.5kV with epitaxial and implanted anode emitter at RT and 400K. The device area is 2.5mm^2.

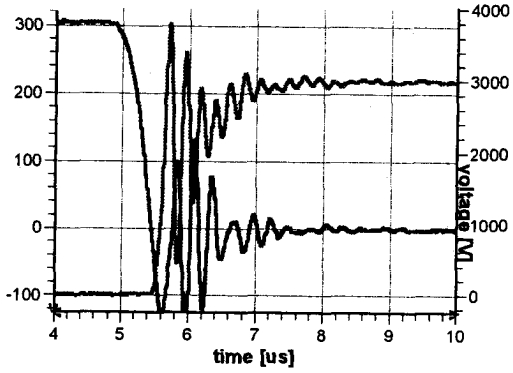

Figure 4 Switching characteristic at Tj=125C of a power module with 8 parallel 4.5kV diodes in a high power circuit. Turn-off at 300Amp, 3000Vdc shows only capacitive reverse recovery. The ringing is due to the very fast transient and circuit/device capacitances.

Dislocations causing the bipolar forward instability in SiC

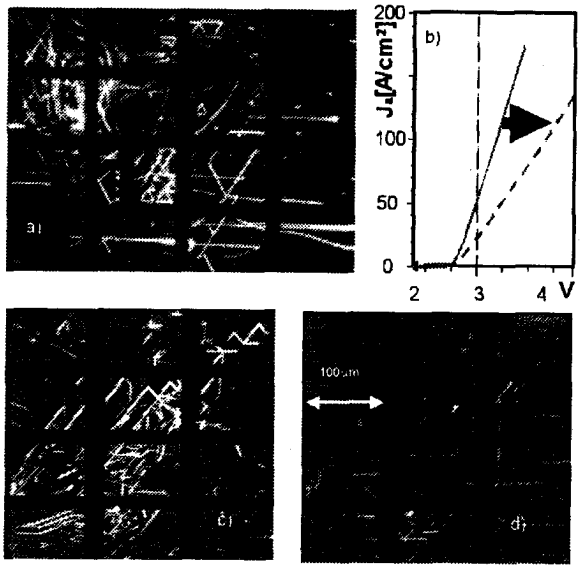

Figure 5 The pictures a), c) show electrically active dislocation maps of virgin epi layers. Dislocation motion creates stacking-faults causing the forward voltage to increase b). In d) the identical area as in c) shows the bounding partial dislocations of the created SF after forward current operation.

defect type	typical dens.	device effect
Micropipes	1-30cm^{-2}	<50 - 70% E_{cr}
Carrots	0.1-10cm^{-2}	E_{cr}, J_L, n
Major pits	1-100cm^{-2}	- , E_{cr}, J_L
Screw disloc.	10^3cm^{-2}	< 80%E_{cr}, τ_{HL}
Edge dislocations	10^4-10^5cm^{-2}	not known
Basal plane disloc.	10^1-10^5cm^{-2}	nucleate ext. SF
Misfit disloc.	0 - 10^3cm^{-2}	nucleate ext. SF
inital small StackFlt	0 - 10^5cm^{-2}	nucleate ext. SF
ingrown StackFault	0 in soa epi	high V_F
Low angle grain boundaries	10^2-10^3cm^{-2}	τ-reduction, forward char.
threading dislocs.	few cm^{-2}	not known
extended stacking faults	0-10^6cm^{-2}	high forward voltage

Table 1 Most common defects in 4H SiC, typical density, and effects on power device characteristics.

Low resistivity ohmic contacts sequentially formed in n- and p-type regions on the same 4H-SiC substrate

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1. Introduction

A widely used technique to form low resistivity ohmic contacts on SiC is to deposit electrode materials such as Ni for the n-type region and layered or alloyed Al/Ti for the p-type region, followed by post-deposition annealing (PDA), typically at 800℃-1000℃ [1]. However, this technique, as is well known, has various drawbacks. PDA causes electrode materials to penetrate the thin n^+ or p^+ layer, to spill over or to attack the field oxide, and markedly degrades electrode surface morphology. This paper proposes an ohmic contact structure and fabrication process that can overcome these issues and are applicable to the manufacture of practical devices, such as JFETs and MOSFETs. It is also shown that specific contact resistances in the range of 10^{-7} Ωcm^2 and $10^{-6}\Omega cm^2$ can be obtained in the n-type and p-type regions, respectively, on (0001) 4H-SiC substrates.

2. Contact Structure and Fabrication Process

Figure 1(i) shows a cross-sectional view of one of the proposed contact, where two different contacts are formed in the source and the gate on a vertical channel 4H-SiC JFET [2] as a example. The major structural features of these contacts are: they are formed on heavily doped n^+/p^+ regions leading to field emission conduction; the contact materials are thin Ni for the source and layered Ti/Al for the gate (the notation Ti/Al means Ti deposition followed by Al deposition); both the contact materials are defined just in the contact windows leaving a constant and fine clearance to the field oxide; and this field oxide consists of a thin thermal oxide and a thick CVD oxide.

Figure 1 outlines the fabrication process of the contact structure. (a) Using selective-area multiple-energy ion-implantation and impurity-activation annealing, the p and p^+ gate regions and the n^+ source region are formed on a vicinal (0001) n^+ 4H-SiC substrate with a lightly N-doped epitaxial layer. (b) The field oxide is grown on the surface by thermal oxidation and atmospheric pressure CVD. (c) Then, contact window is opened in the field oxide over the p^+ gate region by photolithography using a buffered hydrofluoric solution and (d) 80-nm-thick Ti and about 350-nm-thick Al are successively deposited by electron beam evaporation on the surface which still has the photoresist. (e)When the photoresist is lifted off, the well-defined Ti/Al is left on the the bottom of the gate-contact window. (f) In the same manner, 50-nm-thick Ni is defined on the bottom of the source-contact window. (g) Then, after 50-nm-thick Ni is deposited on the back side of the substrate, (h) all the contacts are simultaneously annealed at 1000℃ for 2 min in Ar by rapid thermal annealing. (g) Finally a thick metal over-layer such as Al is deposited on the surface by DC magnetron sputtering and patterned by photolithography using RIE.

3.Results

Ni and Ti/Al contact test structures with the linear transmission line model configuration were fabricated in the heavily N- and Al-doped regions, respectively, on a vicinal (0001) 4H-SiC epitaxial substrate. TLM analysis indicated, as is shown in Fig. 2, that these alloyed contacts had low specific contact resistances of typically 3.3×10^{-7} Ωcm^2 for n-type SiC/Ni and 9.5×10^{-7} Ω

cm^2 for p-type SiC/Ti/Al at room temperature. A 30-min annealing test from 50℃ to 500℃ in 50℃ increments revealed that a significant increase in contact resistance did not occur for either type of contact.

Acknowledgements

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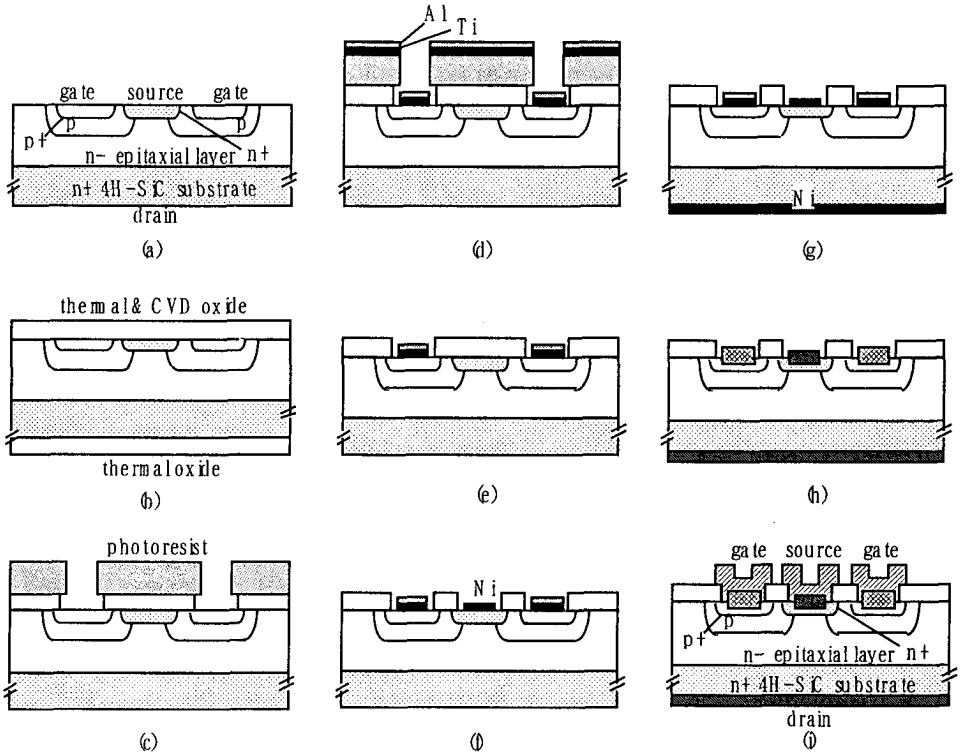

Fig. 1 A fabrication process of proposed contacts combined with JFET structure

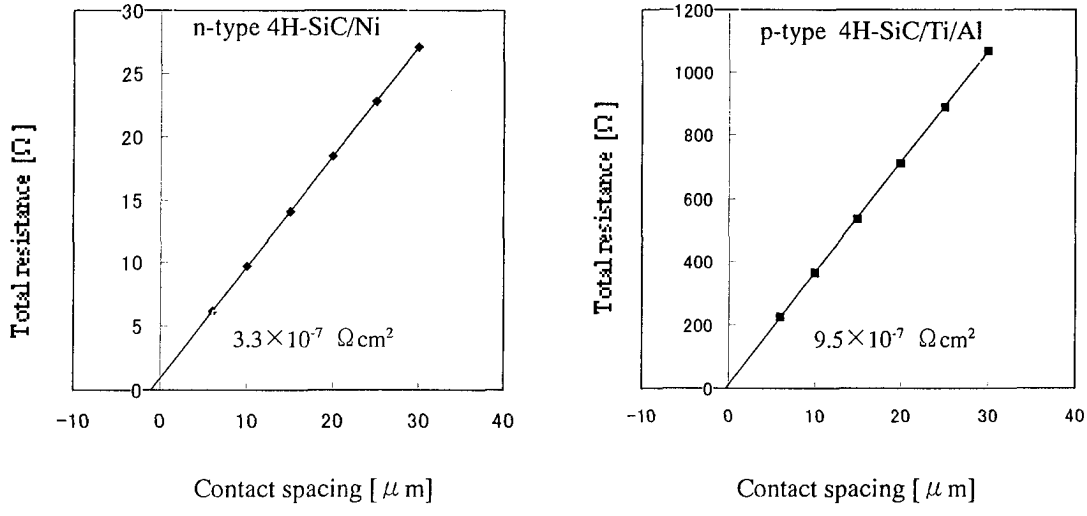

Fig. 2 Plots of total resistance of as a function of contact spacing